Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1. (currently amended) A clock alignment circuit comprising:

a delay line having a plurality of delay elements, wherein each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage, to generate a delayed clock signal with respect to a reference clock signal;

a comparator, coupled to the delay line, to compare the delayed clock signal and the reference clock signal and to output delay differential information, wherein the delay differential information is representative of a correction information between the reference clock signal and the delayed clock signal;

charge pump circuitry, coupled to the comparator, to convert the delay differential information to a control signal, wherein the control signal is proportional to the delay differential information;

A1 cont

an amplifier coupled to the charge pump circuitry, wherein the amplifier includes:

a first input to receive the control signal;

a second input to receive a feedback signal; and

an output to provide the supply voltage and the feedback signal responsive to the control signal~~; and~~

~~a capacitor coupled between the supply voltage and a secondary power supply~~.

2. (currently amended) The clock alignment circuit of claim 1, wherein the ~~first input is a non-inverting input and the second input is an inverting input~~ supply electrode is a transistor source.

3. (currently amended) The clock alignment circuit of claim 1, wherein the ~~delay line includes a plurality of differential delay elements~~ supply electrode is a load electrode source.

4. (currently amended) The clock alignment circuit of claim 1, wherein the ~~delay line includes a plurality of inverter delay elements~~ supply electrode is a pull-up transistor source.

5. (currently amended) ~~The clock alignment circuit of claim 1,~~ A clock alignment circuit comprising:

a delay line having a plurality of delay elements, wherein each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage, to generate a delayed clock signal with respect to a reference clock signal;

A1 cont

a comparator, coupled to the delay line, to compare the delayed clock signal and the reference clock signal and to output delay differential information, wherein the delay differential information is representative of a correction information between the reference clock signal and the delayed clock signal;

charge pump circuitry, coupled to the comparator, to convert the delay differential information to a control signal, wherein the control signal is proportional to the delay differential information;

an amplifier coupled to the charge pump circuitry, wherein the amplifier includes:

a first input to receive the control signal;

a second input to receive a feedback signal; and

an output to provide the supply voltage and the feedback signal;

a capacitor coupled between the supply voltage and a secondary power supply,

wherein the amplifier further includes:

a current mirror load having a first and a second load transistor coupled in parallel, the first and the second load ~~transistor~~ transistors each having a supply electrode coupled to a ~~third~~ first supply voltage;

a bias transistor ~~electrically~~ coupled to a ~~fourth~~ second supply voltage, the bias transistor responding to a bias voltage to provide a bias current at a drain electrode;

a first differential input transistor having a source ~~node~~ coupled to the drain electrode of the bias transistor, wherein the first differential input transistor is coupled in series with the first load transistor; and

a second differential input transistor having a source ~~node~~ coupled to the drain electrode of the bias transistor, wherein the second differential input transistor is coupled in series with the second load transistor.

A1 cont

6. (currently amended) The clock alignment circuit of claim 5, wherein the first and ~~a~~ the second load transistors are PMOS type transistors, the first and the second differential input transistors are NMOS type transistors, the ~~third~~ first supply voltage is a VDD supply voltage, and the ~~fourth~~ second supply voltage is a ground.

7. (currently amended) The clock alignment circuit of claim 5, further including a disabling transistor coupled to a gate electrode of the bias transistor, to disable the bias transistor in response to a disable signal ~~wherein, the disabling transistor in response to a disable signal, disables the bias transistor~~.

8. (currently amended) The clock alignment circuit of claim 5, further including a bias generator to provide the bias voltage, the bias generator includes:

a second current mirror load including a third and a fourth load transistor coupled in parallel, the third ~~first~~ and the fourth ~~second~~ load ~~transistor~~ transistors each having a source ~~node~~ coupled to a ~~fifth~~ third supply voltage;

a third input transistor having a source ~~node electrically~~ coupled to a ~~sixth~~ fourth supply voltage, wherein the third input transistor is coupled in series with the third load transistor; and

a fourth input transistor having a source ~~node electrically~~ coupled to the ~~sixth~~ fifth supply voltage, wherein the fourth input transistor is coupled in series with the fourth load transistor.

A1 cont

9. (currently amended) The clock alignment circuit of claim 8, wherein the third and the fourth load transistors are PMOS type transistors, and the third and fourth input transistors are NMOS type transistors, the ~~fifth~~ third supply voltage is a VDD voltage, and the ~~sixth~~ fourth and the fifth supply ~~voltage is~~ voltages are ground.

10. (currently amended) The clock alignment circuit of claim 1, wherein the comparator includes;

a first pulse generator to generate a first pulse in response to a clock transition of the reference clock signal;

a second pulse generator to generate a second pulse in response to a clock transition of the delayed clock signal; and

a latch circuit to generate a first and a second phase information, wherein in response to a first pulse, the latch circuit generates the first phase information and in response to the second pulse, the latch circuit generates the second phase information.

11. (currently amended) The clock alignment circuit of claim 10, wherein:

the first pulse generator includes a plurality of delay elements coupled to an input of a first logic gate, wherein the first logic gate outputs the first pulse;

the second pulse generator includes a plurality of delay elements coupled to an input of a second logic gate, wherein the second logic gate outputs the second pulse; and

the latch circuit includes a set input receiving the first pulse and a reset input receiving the second pulse.

12. (currently amended) ~~The clock alignment circuit of claim 1,~~ A clock alignment circuit comprising:

A1 cont

a delay line having a plurality of delay elements, wherein each delay element of the plurality of delay elements includes a supply electrode to receive a supply voltage, to generate a delayed clock signal with respect to a reference clock signal;

a comparator, coupled to the delay line, to compare the delayed clock signal and the reference clock signal and to output delay differential information, wherein the delay differential information is representative of a correction information between the reference clock signal and the delayed clock signal;

charge pump circuitry, coupled to the comparator, to convert the delay differential information to a control signal, wherein the control signal is proportional to the delay differential information;

an amplifier coupled to the charge pump circuitry, wherein the amplifier includes:

a first input to receive the control signal;

a second input to receive a feedback signal; and

an output to provide the supply voltage and the feedback signal;

a capacitor coupled between the supply voltage and a secondary power supply,

wherein the charge pump circuitry includes:

a first current source to receive a first supply voltage, the first current source having a control electrode to receive a bias control signal;

a first load transistor coupled to a first reference terminal;

a first input transistor coupled in series between the first current source and the first load transistor, the first input transistor responds to a first phase input to provide a first pump output;

a second current source receiving ~~the~~ a second supply voltage, the second current source having a control electrode to receive the bias control signal;

a second load transistor coupled to ~~the first~~ a second reference terminal, wherein the second load transistor responds to the first pump output;

a second input transistor coupled in series between the second current source and the second load transistor, the second input transistor responsive to a second phase input to provide a charge pump output; and

A1 cont

a current source control coupled between ~~the~~ a third supply voltage and ~~the first~~ a third reference terminal, the current source control includes a control input transistor responsive to the charge pump output and a current source control to provide the bias control signal, wherein the bias control signal is ~~varied in accordance~~ responsive to the charge pump output; and

a capacitor coupled between the charge pump output and a fourth ~~second~~ reference terminal, wherein the charge pump output provides the control signal.

13. (currently amended) The clock alignment circuit of claim 12, wherein the first, second and the third supply ~~voltage is~~ voltages are a VDD voltage, and the first, the second, the third and the fourth ~~and second~~ reference ~~terminal~~ terminals are ~~both~~ a ground terminal ~~terminals~~.

14. (currently amended) The clock alignment circuit of claim 12, wherein the charge pump circuitry further includes:

a third input transistor coupled in series with the first current source, wherein the third input transistor includes a gate electrode ~~which is~~ responsive to a third phase input;

a third load transistor coupled between ~~the first~~ a fifth reference terminal and the third input transistor;

a fourth input transistor coupled in series with the second current source, wherein the fourth input transistor includes a gate electrode ~~which is~~ responsive to a fourth phase input; and

a fourth load transistor coupled between ~~the first~~ a sixth reference terminal and the fourth input transistor.

15. (original) The clock alignment circuit of claim 12, wherein the first and third phase inputs are complementary and the second and fourth phase inputs are complementary.

A1 cont

16. (original) The clock alignment circuit of claim 1, further including a multiplexer circuit and an interpolator circuit, wherein the supply voltage is provided to the multiplexer circuit and the interpolator circuit.

17. (currently amended) A power supply generator for generating a first supply voltage for clock alignment circuitry wherein the clock alignment circuitry includes a delay line having a plurality of delay elements, each delay element of the plurality of delay elements includes a source electrode to receive the first supply voltage, the delay line generating a delayed clock using a reference clock, the clock alignment circuitry further including a comparator to detect a correction information between the delayed clock and the reference clock to generate error information representative of the correction information, and a charge pump to convert the error information into a control signal, wherein the control signal is proportional to the error information, the power supply generator comprising:

an operational amplifier having an output to provide the first supply voltage, wherein the operational amplifier includes:

a bias transistor biased by a bias voltage;

a differential amplifier coupled to the bias transistor, wherein the differential amplifier includes a first differential input to receive the control signal and a second differential input coupled to the output in ~~a non-inverting~~ <u>an inverting</u> configuration;

a bias generator to provide the bias voltage, the bias generator having a first input coupled to the control signal and a second input to receive the bias voltage;

wherein, in response to the control signal, the bias generator provides ~~a~~ <u>the</u> bias voltage ~~which is~~ representative of a change in the control signal; and

a capacitor coupled between the output and a supply terminal.

A1 cont

18. (currently amended) The power supply generator of claim 17, wherein the differential amplifier further includes:

a <u>first</u> current mirror load circuit having a first and a second <u>load</u> transistor coupled in parallel, the first and <u>the</u> second <u>load</u> transistors each having a source electrode coupled to a ~~third~~ <u>second</u> supply voltage;

a first input transistor having a source electrode coupled to a drain electrode of the bias transistor, <u>wherein</u> the first input transistor <u>is</u> ~~being~~ coupled in series with the first load transistor and responsive to the first differential input; and

a second input transistor having a source electrode coupled to the drain electrode of the bias transistor, <u>wherein</u> the second input transistor <u>is</u> ~~being~~ coupled in series with the second load transistor and responsive to the second differential input.

19. (currently amended) The power supply generator of claim 18, wherein the first and the second transistors are PMOS type transistors, the first and the second ~~differential~~ input transistors are NMOS type transistors, the ~~third~~ second supply voltage is a VDD voltage~~, and the fourth supply voltage is a ground voltage.~~ and a third supply voltage is coupled to the bias transistor, wherein the third supply voltage is a ground.

20. (currently amended) The power supply generator of claim 19, wherein a channel width of the first load transistor and a channel width of the second load transistor are sized such that, when in operation, the first and the second load ~~transistor~~ transistors are in a saturated mode.

A1 cont

21. (original) The power supply generator of claim 17, further including a disabling transistor, coupled to the gate of the bias transistor, to disable the bias transistor in response to a disable signal.

22. (currently amended) The power supply generator of claim 18~~17~~, wherein the bias generator further includes:

a second current mirror load circuit having a ~~first~~ third and a ~~second~~ fourth load transistor coupled in parallel, the third ~~first~~ and ~~second~~ the fourth load transistors of the second current mirror load circuit each having a source electrode coupled to a ~~fifth~~ third supply voltage;

a third input transistor having a source electrode ~~electrically~~ coupled to a ~~sixth~~ fourth supply voltage, wherein the third input transistor is coupled in series with the third load transistor, wherein the third input transistor includes a gate electrode to receive the control signal; and

a fourth input transistor having a source electrode ~~electrically~~ coupled to the ~~sixth~~ fifth supply voltage, wherein the fourth input transistor is coupled in series with the fourth load transistor.

23. (currently amended) The power supply generator of claim 22 wherein the first, the second, the third and the fourth ~~and second~~ load transistors are PMOS type transistors, the first, the second, the third and the fourth input transistors are NMOS type transistors, the ~~fifth~~ second and the third supply ~~voltage is~~ voltages are a VDD voltage, and the ~~sixth~~ forth and fifth supply ~~voltage is~~ voltages are a ground ~~voltage~~.

24. (currently amended) The power supply generator of claim 22, wherein the bias generator further includes a disabling transistor coupled to the second current mirror load circuit, to disable ~~the~~ a second current mirror bias.

A1 cont

25. (original) The supply generator of claim 17, wherein the clock alignment circuitry includes a delay lock loop.

26. (currently amended) A method of generating a supply voltage for use in clock compensation circuitry, the clock compensation circuitry includes a plurality of delay elements in a delay line and receives a clock signal, the method comprising:

providing a supply voltage to a ~~common~~ source of a transistor in a delay element ~~electrode~~ of the plurality of delay elements;

providing a delayed clock signal using the delay line, the delayed clock signal having a time delay with respect to the clock signal;

detecting a delay skew between the delayed clock signal and the clock signal;

converting the delay skew to a voltage signal wherein the voltage signal is proportional to the delay skew; and

generating the supply voltage by an amplifier responsive to the voltage signal~~tracking the voltage signal using an amplifier to generate the supply voltage~~.

27. (original) The method of claim 26, wherein the delayed clock signal is provided by propagating the clock signal through the plurality of delay elements and tapping an output of one of the delay elements from the plurality of delay elements.

28. (original) The method of claim 26, wherein detecting the delay skew includes:

generating a first pulse in response to a clock signal edge of the clock signal, wherein the clock signal edge of the clock signal occurs at a first time;

generating a second pulse in response to a clock signal edge of the delayed clock signal, wherein the clock signal edge of the delayed clock occurs at a second time, and wherein the second time occurs after the first time to define a period representative of the clock skew;

A1 cont

setting a latch circuit using the first pulse; and

resetting the latch circuit using the second pulse, wherein the latch circuit outputs first delay skew information during the period.

29. (original) The method of claim 26, wherein detecting the delay skew includes:

generating a first pulse in response to a clock signal edge of the delayed clock signal, wherein the clock signal edge of the delayed clock signal occurs at a first time;

generating a second pulse in response to a clock signal edge of the clock signal, wherein the clock signal edge of the clock signal occurs at a second time, and wherein the second time occurs after the first time to define a period representative of the clock skew;

resetting a latch circuit using the first pulse; and

setting the latch circuit using the second pulse, wherein the latch circuit outputs second delay skew information during the period.

30. (currently amended) ~~The method of claim 26,~~ A method of generating a supply voltage for use in clock compensation circuitry, the clock compensation circuitry includes a plurality of delay elements in a delay line and receives a clock signal, the method comprising:

providing a supply voltage to a common source electrode of the plurality of delay elements;

providing a delayed clock signal using the delay line, the delayed clock signal having a time delay with respect to the clock signal;

detecting a delay skew between the delayed clock signal and the clock signal;

converting the delay skew to a voltage signal wherein the voltage signal is proportional to the delay skew; and

tracking the voltage signal using an amplifier to generate the supply voltage,

A1 cont

wherein the amplifier includes a differential amplifier biased by a current source, the differential amplifier including a first input, a second input and an output to provide the supply voltage, wherein tracking the voltage signal includes:

receiving the voltage signal at the first differential input;

applying the output to a second differential input;

amplifying a voltage differential between the first input and the second input;

biasing the current source with a bias signal; and

generating the supply voltage at the output, wherein the supply voltage is proportional to the voltage differential.

31. (currently amended) The method of claim 30, wherein the amplifier further includes a bias generator having a first input, a second input, and an output to provide the bias signal, and wherein biasing the current source includes:

receiving the voltage signal at the first input;

applying the output to the second input;

amplifying a voltage differential between the first input and the second input; and

A1 cont'd

generating the bias signal at the output, wherein the bias ~~voltage~~ signal is proportional to the voltage differential.